Design of Low Power Static Contention-free Flip Flop using 18nm finFET Technology

DR. ASIYA SULTHANA[1], M. A. MUDASSIR AHMED[2]

[1]Associate Professor, Department of ECE, Vaagdevi College of Engineering, Telangana, India.

[2]Department of ECE, Vaagdevi College of Engineering, Telangana, India.

[1]asiyasulthana@vaagdevi.edu.in, [2]mudassirahamed@vecw.edu.in

ABSTRACT

This work describes a Low Power static contention-free flip-flop (LPSCFF) which has been made in 18nm FinFET technology. The architecture is optimized to provide low power usage and switching latency of sub-nanosecond and still provide fully-static operation. The circuit topology has conditional evaluation logic and standardised device dimensions to remove parallel concurrent conduction paths of pull-up and pull-down components. This method will ensure a consistent operation over a broad range of process, voltage temperature (PVT) conditions. At 0.8 V, the simulation results indicates an average power of 1.83 uW and a delay of 241.5 ps which translates to a power-delay product of 0.44 fJ. The robustness of delay and power usage characteristics is tested by a thorough analysis of a range of supply voltages (0.7 to 0.9 V), a temperature range between -50°C to 75°C and key process corners. The proposed design has over 80% PDP improvement over other recent 18-nm FinFET flip-flops, and is also much faster, and is highly appropriate to contemporary low-power, high-performance digital systems.

Keywords—*static contention-free flip-flop, 18nm FinFET technology, PVT*

I. INTRODUCTION

Sequential storage elements still play a decisive role in the determination of the overall timing and energy behaviour of synchronous integrated circuits. As the fabrication nodes have progressed to sub-18 nm FinFET, nanosheet regimes, the designers have been confronting more and more of the issues like Clock Induced Switching Current, degraded noise margins, and higher susceptibility to supply variations. These problems become particularly critical in flip-flop structures where there is often rapid charge redistribution within internal nodes of the circuit during the clock transitions which often gives rise to overlap conduction between pull-up and pull-down devices. Conventional transmission gate flip flops and C²MOS latches are reliable when they are run at moderate speeds. However they have a tendency to have quite a high short circuit power dissipation and timing uncertainty under aggressive voltage scaling [1].

To achieve better robustness and to minimize the dynamic part of energy consumption, more recent works are more focusing on the data aware sequential circuits that only activate the evaluation paths when the input transition is meaningful. Several methods of conditional-transfer and conditional-capture strategies have been investigated in order to minimize redundant switching, but many of which involve the use of dynamic storage nodes that need to be refreshed consistently for proper operation, or are subject to leakage of their charge at low frequencies [2]. Similarly, pulse triggered flip flops have good speed-power trade-offs but have narrow transparency windows and are more sensitive to device mismatch for implementation in advanced node [3]. Static feedback based structures have been introduced to obtain better state retention, but they contribute to long intervals of contention during the clock overlap period, which limits the effectiveness in low power and high frequency environments [4].

These limitations point to the need for a flip flop architecture with both static data retention, non-overlapping conduction and contention-free switching. Motivated by this need, this work presents a Low Power Static Contention-Free Flip-Flop (LPSCFF) which avoids the short-circuit overlap by controlling the discharge and charging paths via the conditional transistors using data dependency. The flip flop comprises of two complete static latching stages and controlled feedback strength. This design will ensure that a NMOS and PMOS devices are no longer driving the similar internal node instantaneously. This approach provides a means of reliable operation under voltage scaling, provides better noise immunity and substantially ameliorates the power of short circuits. The proposed LPSCFF is thus a good candidate for energy efficient sequential logic in next-generation digital processors, embedded controllers and mixed-signal SoC operating over large PVT conditions.

II. LITERATURE SURVEY

Sequential building blocks still represent a significant fraction of a power budget and timing margin in highly scaled digital systems and the development of robust and energy efficient flip-flops has been a research focus in the recent VLSI literature. This means that as the size of the geometries of devices decreases, as supply voltages come down, internal storage nodes become more susceptible to overhead currents and overlap effects induced by the clock. An initial experiment on low-power static flip-flops has

noted that traditional transmission-gate and C²MOS designs continue to permit the short periods of simultaneous pull-up and pull-down conduction, in particular, during the evaluation and recovery phases of the clock, which exacerbates the amount of short-circuit energy and reduces stability under scaled supply conditions [5]. Further developments of FinFET and nanosheet devices claimed that the internal latch node-based transitions are dominated by parasitics, which enhance contention-induced losses, which led to the development of device-sensitive sequential architecture development [6].

Some of the researchers have sought to deal with these related weaknesses by considering compact static flip-flops, minimising the number of transistors and the complexity of the clocking network. NOR based master slave stages or inverter compressed path designs have been proven to provide area and clock-load reduction, and at a low power factor have demonstrated competitive delay [7]. These solutions enhance the layout efficiency but research has indicated that even the internal regeneration paths still suffer an overlap conduction during switching particularly when input switches near the sampling time, which constrains their ability to support aggressive voltage scaling [8].

Conrad's other prospective future has been the conditional-evaluation and data-aware flip-flops. These works repress redundant internal transitions by allowing discharge or charge paths to be made only when an important input change takes place. With low-input activity factors, such conditional-capture or conditional-transfer schemes are effective in reducing the switching activity and also enhancing energy behaviour [9]. Though they are power-efficient designs, most of them tend to include semi-dynamic nodes or precharge-evaluate steps that are susceptible to leakage, charge loss and duty-cycle distortion especially during long idle times or during near-threshold operation [10].

The same has been investigated by parallel developments looking at pulse-triggered flip-flops, which use slender clock pulses to minimize the quantity of internal storage nodes and decrease the critical paths. The most recent pulse-triggered models add compact pulse sources, feedthrough-enhanced data routes and gated pull-up networks to enhance energy-demand figures [11]. Such designs however rely very much on a uniform pulse-width over PVT corners. Fluctuations in the produced pulse are a cause of concern in the aspect of hold-time failures, race-through and metastability and thus such designs are sensitive to device mismatch and clock skew [12]. Even though pulse-triggered flip-flops can perform very well in nominal conditions, their dynamic behaviour reduces their reliability in the long-term in low-voltage and high-variation conditions.

A second trend has been on dual-edge triggered flip-flops which achieve lower global clock frequency requirements by measuring data on both clock edges. Recent dual-edge designs have symmetrical evaluation paths and redundant-transition-suppression to minimize internal power consumption [13]. These techniques reduce the real clock switching energy, but add more internal nodes and control signals and make the structure of the latches more complicated and the potential momentary contention higher.

Third, the vast majority of designs that have good nominal power-delay behaviour do not have good scaling behaviour with voltage and variation in process, primarily because they rely on dynamic behaviour, there are a large number of internal transitions or complex control paths.

More recently, designers are starting to respond explicitly to reduction of contention. There are also modern non-static flip-flops which have clock-controlled gating circuits within the regeneration path to avoid simultaneous pull-up and pull-down activation [14]. Phased clock decoupling, or the selective disconnection of internal branches is used by others to reduce overlap currents [15]. Most of these techniques have still short latencies where pairs of devices can be left co-operating during transition, particularly when the input to the devices varies quickly, or when there is a change in the clock-slope. Similarly, those solutions that rely on dynamic or precharge phases offer partial contention control capability, but cannot afford to maintain a static retention without a refreshing period, and so are weak in severe PVT corners [16].

The latest efforts on dual-edge triggered flip-flops are still trying to balance between power, delay, and strength through various structural methods. The STC-DET flip-flop in Figure 1 demonstrates that the flip-flop operates on a static clocking which captures the input data on dual edges via its complementary latches. It retains data efficiently but needs a dual phase clock, which can load clocks [17]. To make the clock simpler, the TSPC-SDET flip-flop in Figure 2 is deployed to a unit phase TSPC architecture. It has a dynamic precharge and dynamic evaluation, is capable of operating on two edges and its dynamic node renders it leakage sensitive and unstable at low frequencies [18]. Figure 3 is a more recent design, the LPLD-DET flip-flop, which is more delay and energy efficient, requiring fewer clocked transistors. It also operates conditional discharge, and a fixed keeper, but short pull-up/pull-down overlap still causes full removal of contention [19]. These designs demonstrate a gradual improvement of DET architectures, and points to ongoing issues of dynamic-node vulnerability, clock overhead, and partial contention, which motivate efforts to find more robust, contention-free, designs.

In the literature provided above, three research gaps are identified. To start with, a good percentage of energy-

efficient solutions are semi-dynamic, which is susceptible to leakage, charge-sharing and pulse-width distortion in nature. Fully static structures with high retention are restrained.

Second, there are very few designs with full contention elimination at all the internal nodes under all clock conditions. The majority of existing solutions minimize, though do not eliminate, the concomitant conduction between pull-up and pull-down networks.

Third, most designs with good nominal power-delay behaviour do not scale well to voltage and process variation, mainly due to their dependence on dynamic behaviour, numerous internal transitions or complicated control paths.

These shortcomings explain the importance of a flip-flop that is able to store fully static, with a strict non-overlapping conduction, as well as resistant behaviour to PVT variation, without depending on pulse generation or dynamic precharge. These observations inspire the current work, in which a contention free flip-flop, which is not active, is proposed by reformulating the internal discharge and retention network using data-dependent conditional devices such that the internal nodes are never concurrently driven by the competing transistor networks. This design fills the weaknesses that have been recognized in the previous designs and offers a stable low-power design applicable to advanced technology nodes.

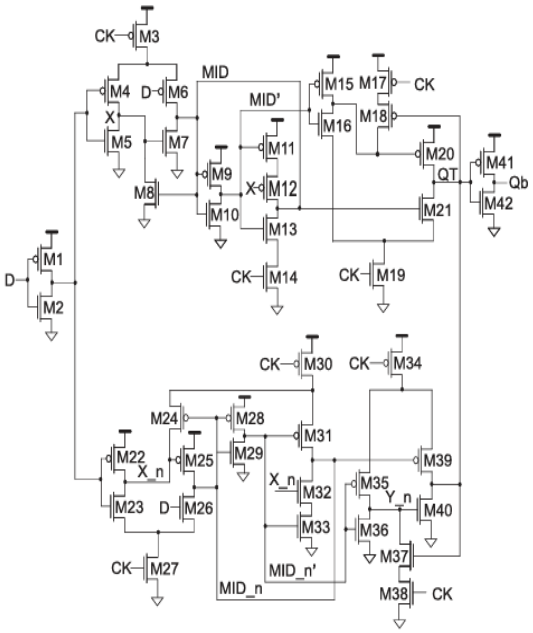


Figure 1: Circuit of the STC-DET flip-flop [17]

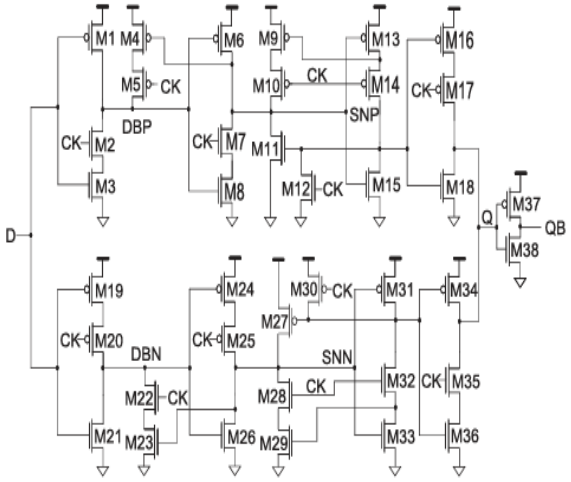


Figure 2: Circuit of the TSPC-SDET flip-flop [18]

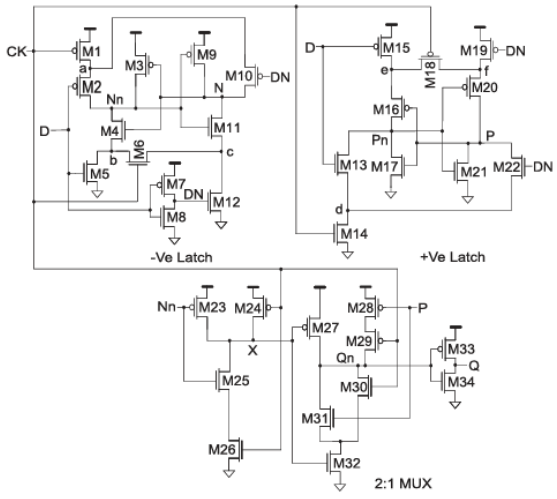
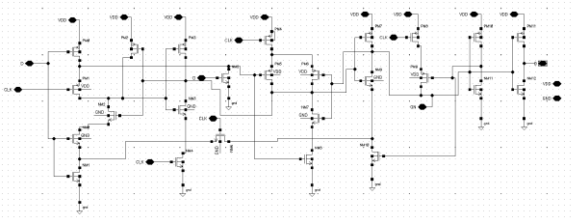


Figure 3: Circuit diagram of the LPLD-DET flip-flop [19]

III. Proposed Low Power Static Contention-Free Flip-Flop (LPSCFF)



The proposed Low Power Static Contention-Free Flip-Flop (LPSCFF) circuit which combines a completely static storage with contention-free switching mechanism is shown in Figure 4. "Static" means the flip flop retains its logic state indefinitely, and the flip flop does not require periodic precharging and refreshing as dynamic and TSPC designs. Weak feedback keepers are used to hold the internal nodes, which means that they allow for stable data to be maintained at low frequencies or when the clock is

gated. "Contention-free" refers to the elimination of short term currents that occur when pull-up and pull-down networks conduct simultaneously at the same node during a clock transition. In typical transmission-gate flip-flops, such overlap just wastes power and ruins performance. The LPSCFF avoids this through the use of conditional evaluation and isolation transistors which are only activated when their complementary devices are perfectly off. Thus, all internal nodes are charged/discharged by only one network at a time, ensuring conflict free switching.

Figure 4: Design of Proposed Low Power Static Contention-Free Flip-Flop (LPSCFF)

Structurally, the LPSCFF consists of two connected in cascade latch, namely master and slave latch. Each latch is based on cross coupled inverters using conditional data paths. The clock alternately allows the latches: the master takes input data on the low phase, and the slave passes on the input to the output on the high phase. Because both latches are static and isolated using non-overlapping control signals, the design has a high robustness, low power consumption and immunity to charge sharing/leakage.

The name Static Contention-Free Flip-Flop provided a good description of its dual characteristics of static data retention and contend free operation that collectively will lead to better power-delay performance over conventional flip flop architectures.

The LPSCFF has twelve PMOS transistors (P1 to P12) and twelve NMOS transistors (N1 to N12) divided into two latch stages; the master latch and the slave latch. The master latch is driven by the clock (CLK), and it catches the input data whenever the clock signal ticks low. The slave latch whose clock is complementary CLK- is responsible for generating the final output - Q when the clock is high. Conditional evaluation transistors like N3, N4, N7 and N8 are gated by the data input and complementary internal node signals, that is, discharging occurs only when logically required and there is no direct contention between pull up and pull down paths. The cross coupled inverter pairs (P5-N5-P6-N6 in the master and P9-N9-P10-N10 in the slave) are used as bistable storage elements and the weak feedback devices (P11-N11 and P12-N12) used to reinforce the logic levels stored in the bistable storage elements for static data retention. The clock signal alternately enables and disables conduction paths between the master and slave sections so that data propagation and storage takes place in two separate and non-overlapping clock phases.

A. Circuit Operation

The behavior of the LPSCFF can be best understood by examining the behavior of the LPSCFF in the four key clock and data configurations. There are two cascaded latches in the circuit, one is the master latch and other is the slave latch. The transistors P1 to P6 and N1 to N6 constitute the master latch and the transistors P7 to P12 and N7 to N12 the slave latch. The clock alternately turns on one of the latches and turns off the other. Data is evaluated in the master latch and then is stored in the slave latch. Special discharge and keeper transistors in each latch ensure that no more than one current path is active at a time which prevents static contention and power short circuits.

Case 1: CLK = 0 & D = 0. If the clock is low, then master latch is active and slave latch is isolated. In the master latch, the NMOS N2 is switched off and the PMOS P2 is switched on and hence the internal node X charges into a logic 1. The discharge transistor N3 is switched off because its gate is low and therefore no current is allowed to flow to ground. The weak keeper transistor N4 makes the voltage on node X stable, so that there is no leakage. In this case the high clock, transistors N7 and P7 will remain off and node-Y will maintain its previously latched value through the feedback inverter pair (P9-N9). Thus, the master tracks the input but the slave holds its previous state, with no pull up versus pull down network contention.

Case 2: CLK = 0, D = 1. With a high input of data and a low clock, N2 conducts and P2 is off. This turns ON the discharge transistor N3 which pulls node X towards ground which stores a logic 0. Pull up device P3 remains off and therefore discharging happens with no competing VDD path. Keeper transistor P4 fixes the low level in node X so that it will not drift in voltage. The slave latch is then isolated, N7, P7 are in a non conducting state so the slave holds its previous state. The master samples the high input as a low on node X, which results in contention free switching.

Case 3: CLK = 1, D = 0. When the clock goes high, the master latch is put into an opaque state and stores its stored value on node X through the cross coupled inverter pair (P5-N5 and P6-N6). At the same time the slave latch is made transparent via N7 and P7, so that the value on node X can be transferred to node Y. In case of D = 0, logic 1 from the previous phase is retained at node X. N8 is on and P8 is off, hence at node Y a path to ground through N9 is created, and node Y is pulled to logic 0. The pull up network (P9-P10) will remain off to avoid conflict. The output inverter (P11-N11) drives Q = 0. No simultaneous conduction confirms contention-free data transfer.

Case 4: CLK = 1, D = 1. With high clock and high data input the master latch holds the node X at logic 0 with the help of feedback pair (P5-N5 and P6-N6). The slave latch gets transparent and takes the value via their transmission pair (N7-P7). Since node X = 0, N8 remains off and P8 conducts charging node Y to VDD through the pull up path (P9-P10). The output inverter (P11-N11) produces the output Q = 1. The weak feedback pair (P12-N12) keeps the high level on node Y after the clock drops so as to retain the data for the next cycle. In this case the slave latch does

not have current contention and it does propagate correctly the master value.

What is important in all these 4 scenarios is that the low clock phase renders the master latch transparent and it can track the input while the slave latch retains its value. During the high clock phase, the master latch is isolated and the data is stored in and the output is driven by the slave latch. Conditional evaluation transistors ensure that there is never any chance of pull-up and pull-down paths ending up in contention, eliminating static contention. Keeper transistors are used to make nodes stable against either leakage or noise. This sequential, non-overlapping conduction mechanism provides process independent, temperature independent operation, improved power efficiency, noise margin and speed compared to traditional designs.

IV. Simulation Results

The design of the proposed flip-flop was fabricated by the 18 nm FinFET technology model and all simulations at the device level were done with uniform transistor sizes, where NFET transistor was 2/1 and PMOS transistor was 4/1 to keep the switching properties equal to each other. Functional and timing tests were done at a nominal operating point of 0.8 V and 27°C. A more comprehensive PVT analysis was obtained by operating the supply voltage between 0.7 V and 0.9 V and the temperature range between -50°C and 75°C with slow-slow, typical-typical, and fast-fast process corners. This methodical test gives information into voltage scale, thermal resilience, and process susceptibility of the design in circumstances that would replicate advanced nanometer technology node circumstances.

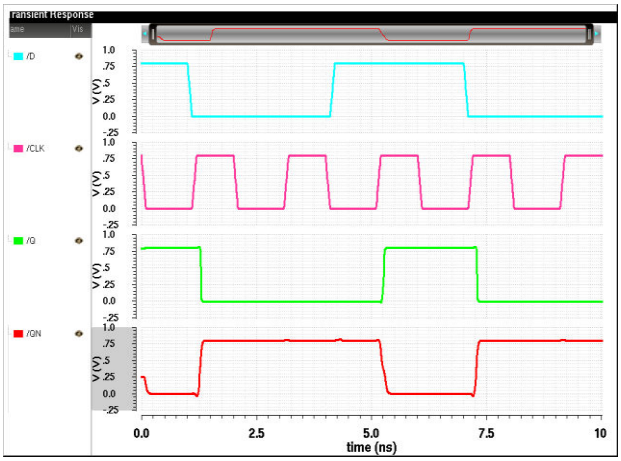


Figure 5: Transient response of the proposed LPSCFF

Figure 5 indicates the transient response of the proposed flip-flop to show the functional behaviour of the flip-flop under the nominal operating conditions. Applied data waveform data has a low high low transition sequence, with the clock signal having a periodic pulse pattern alternating between the transparent and latching phases of the circuit. At times when the clock is low the master stage is transparent and the internal node is able to track the input data. This behaviour is mirrored in the waveform, in which the output is constant until the respective sampling edge is reached. When the clock moves to the high level, the master latch goes opaque and the slave stage takes the value initially stored and the transition at the output node Q becomes clean and stable.

The Q waveform exhibits the appropriate performance of edge-triggered behavior and the variations in the output only at the designated sampling points depending on the clock phase. The complementary output QB shows the complementary inverse switching behavior and is in phase opposition over the whole time of the simulation. Both the Q and QB show full swing voltage levels without distortion, which proves that there is sufficient drive strength on the static latch and sufficient regeneration on the cross-coupled inverters. No glitching or metastable behavior is visible at the clock transitions and this implies that the isolation between the slave and master stages is appropriate and there is no internal contention. The proper functionality and the stability of the retention of the logic levels in the correct state at the logic level of the simulated interval are confirmed by the clean signal transitions and well-defined logic levels across the simulated interval of the flip-flop at nominal biasing conditions.

A. PVT Analysis

1) Process Variation

Process-corner analysis indicates that the flip-flop of Figure 6 is functional at every corner of the simulated corner. With the current devices their propagation delay is approximately 211 ps which is the quickest at the fast-fast (FF) corner with an average power of around 2.0 µW. The slow-slow (SS) corner uses the least power of approximately 1.7 µW, but has the longest delay of approximately 345 ps, which is equal to the lower transistor mobility. Between these extremes are typical-typical (TT), slow-fast (SF) and fast-slow (FS) corners, where delays range over a range of about 225-245 ps with the power in the range of 1.8-2.0 µW. The low dispersion in both measures shows that the contention-free structure does not alter either timing or power properties even when the skew in the process of the contention is high.

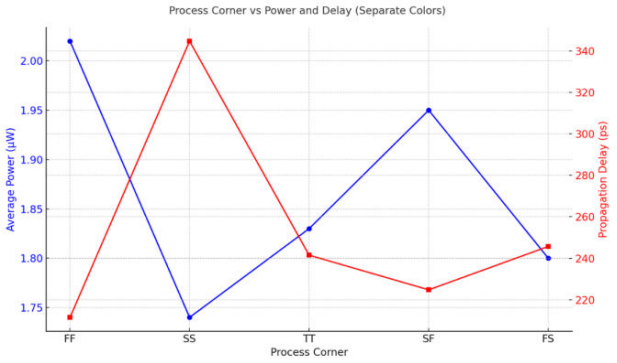


Figure 6: Process Variation of Proposed LPSCFF w.r.t Power Usage and Delay

2) Voltage Variation

The desired trade-off between power consumption and performance is observed by ramping the supply voltage of the flip-flop of Figure 7 between 0.9 V to 0.7 V. The flop has a maximum power at 0.9 V of just under 2.8 µW, but has a delay of less than 230 ps, indicating a good drive capability. This gives a power of approximately 1.8 µW at a dropped voltage of 0.8 V with the delay only slightly increased to nearly 240 ps. Another cut of power to 0.7 V reduces it to about 1.4 µW, but now the waiting period is almost 400 ps. At reduced supply of 0.6 V, the delay goes into the nanosecond range, meaning that it can still be operated near-threshold, albeit at a large timing price. The overall results indicate that the flip-flop is reliable at a voltage of between 0.7 V to 0.9 V with a tradeoff of dynamic voltage response and power delay that is predictable.

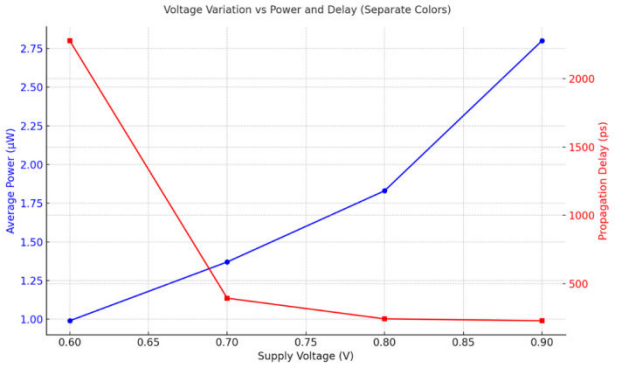


Figure 6: Supply voltage Variation of Proposed LPSCFF w.r.t Power Usage and Delay

3) Temperature Variation

Figure 8 illustrates a temperature scan of the proposed flip-flop between -50°C and 75°C, showing the combined effect of carrier mobility and leakage on the performance of the proposed device. Low temperature operation consumes approximately 1.6-1.7 µW and has a delay of 270-290 ps. When temperature is increased, average power increases to approximately 2.1 µW at a temperature of 75°C due to increased subthreshold and gate leakage; delay reduces to approximately 230 ps as mobility improves and the effective threshold is reduced. As both delay and power vary monotonically, the topology exhibits no interesting anomalous behaviour, such as there being any sudden delay drops, or any switching becoming unstable with thermal stress, which is why it is found to be reliable over a wide ambient temperature range.

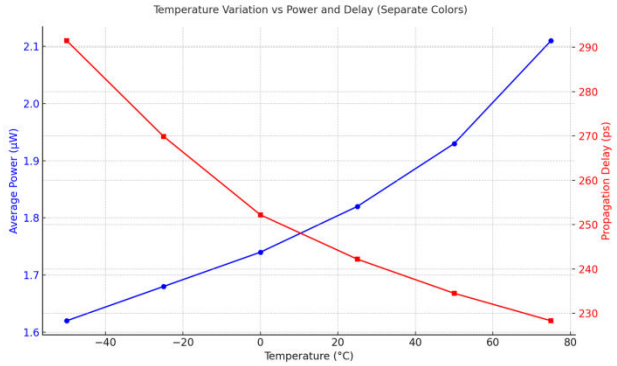


Figure 7: Temperature Variation of Proposed LPSCFF w.r.t Power Usage and Delay

B. Monte Carlo Analysis

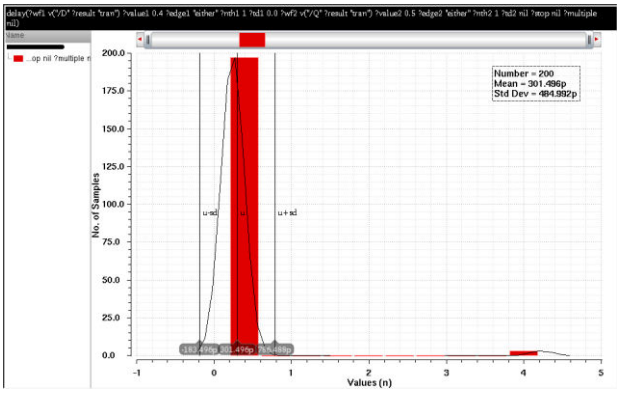


Figure 8: Monte Carlo Analysis of Delay for the Proposed LPSCFF

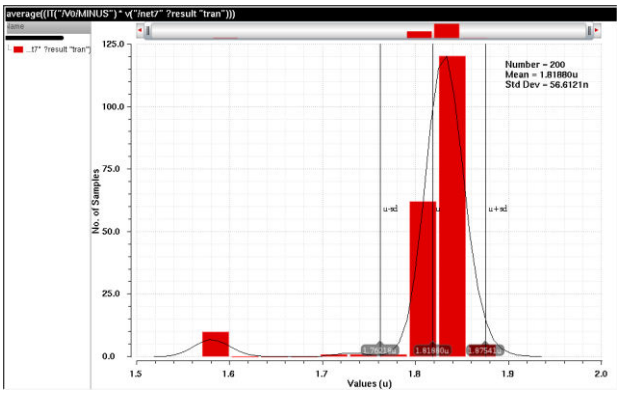


Figure 8: Monte Carlo Analysis of the Power usage for the Proposed LPSCFF

The evaluation of the Monte-Carlo distributions for 200 runs was done based on three-sigma (3σ) statistical limit, which is the 99.7% of all possible variations based on normal devices mismatch. In the case of the delay distribution, the mean of 301.49 and a standard deviation of 484.99 give a 3σ range computing the slowest and fastest probable switching behaviour due to threshold and mobility variation in the 18nm FinFET process as in Figure 8. Though the range of spread of delay is broad, but all samples lie within this statistical envelope, implying predictable timing behaviour with random variations. The distribution of power is also much less deviated, mean of 1.8188 µW and standard deviation equals 56.61 nW shows a much smaller deviation as in Figure 8. It proves the fact that the contention-free structure does not alter the power features in the situation of mismatch very much. The analysis thus confirms that the timing and power is within the anticipated statistical operating range of nanoscale technology.

The Monte-Carlo distributions were evaluated using the three-sigma (3σ) statistical limit, which represents 99.7% of all expected variations under normal device mismatch. For the delay distribution, the mean value of 301.49 ps and standard deviation of 484.99 ps define a 3σ range that captures the slowest and fastest likely switching behaviour arising from threshold and mobility fluctuations in the 18 nm FinFET process. Although the delay spread is wide, all samples fall within this statistical envelope, indicating predictable timing behaviour under random variations. The power distribution shows a much smaller deviation, with a mean of 1.8188 µW and a standard deviation of 56.61 nW, and the corresponding 3σ band remains narrow. This confirms that the contention-free structure maintains highly stable power characteristics even under mismatch. The 3σ analysis therefore verifies that both timing and power remain within the expected statistical operating limits for nanoscale technology.

C. Comparative Analysis

A comparative study was conducted using the latest 18 nanometer FinFET based flip flop designs in order to test the effectiveness of the suggested design which is static and contention free. The classic example of a master slave D flip-flop as described by Venkata Rao et al. [20] states that simple technology scaling to 18nm does not necessarily imply that the device operates with low energy; the experimentally determined power usage is 95% higher and the delay is 20 times more than proposed flip-flop. A hybrid-logic flip-flop, which was shown to operate with moderate power savings with a lower supply voltage, such as the transitional hybrid-logic flip-flop by Jaya Prakash et al. [21], has a clock-to-Q delay exceeding 10ns (due to ratioed evaluation paths) and its power-delay product (PDP) is significantly larger than is ideally required in high-speed circuits.

Table 1: Comparative Analysis of Proposed Flip-flop w.r.t Existing Flip-flops

Reference	Technology (nm)	Avg. Power	Delay	PDP
[20]	18	841.2 µW	5.06 ns	4.26×10^3 fJ
[21]	18	232.2 nW	10.3 ns	2.39 fJ
[22]	18	3.42 µW	3.18 ns	10.87 fJ
Proposed flip-flop	18	1.83 µW	241.5 ps	0.44 fJ

An 18nm FinFET flip-flop based on pass-logic, which is reported by Mohammed Sabeeha et al. [22], has a further reduction in switching power, however, there is delay degradation because of series-connected pass elements. Unlike the current approaches, the proposed flip-flop attains full static, does not have contention paths internally, and has its delays under the nanosecond range and the dynamic power requirement of just a few microwatts, which translates into a significantly lower PDP and a more favorable energy-performance trade-off. The suggested, contention-free, flip-flop, on the other hand, is capable of reducing power-delay product by approximately 80-90% with a reduced or sub-nanosecond latency, which is significantly more efficient than the current system based on FinFET technology.

V. Conclusion

It is demonstrated that a contention-free static flip-flop can provide powerful energy-performance in state-of-the-art FinFET nodes. This is done through the proper coordination of the internal discharge and retention paths. The design is based on a uniform transistor size, removal of overlap current, and retention of fully stationary storage to ensure that the behaviour of the design is constant with voltage, temperature, and variation in process. When conditions are nominal, the design attains power-delay product (PDP) of 0.44 fJ. These are many times better than recently published 18nm FinFET flip-flops, which have either multi-nanosecond delays or high dynamic power. The results obtained prove that the given architecture can be used in power-restricted logic in high-speed FinFET-based SoCs. It has a small, energy-efficient solution compared with the current static, hybrid, and pass-logic designs.

References

[1] K. Rao, M. Takamiya, and T. Sakurai, "Energy and timing reliability of sequential cells in advanced FinFET technologies," IEEE Trans. Circuits Syst. I, vol. 67, no. 10, pp. 3598-3610, 2020.

[2] F. Martins and R. Reis, "Data-aware sequential circuits for reduced switching in ultra-low-power logic," Integration, the VLSI Journal, vol. 82, pp. 31-42, 2021.

[3] H. Arima, Y. Shinohara, and K. Kuroda, "Pulse-triggered storage elements with enhanced variation tolerance for deep-submicron CMOS," IEEE Trans. VLSI Syst., vol. 30, no. 5, pp. 742-754, 2022.

[4] D. Shin and J. Park, "Static latch architectures with strengthened retention for nanoscale digital systems," IEEE Access, vol. 10, pp. 113428-113439, 2022.

[5] A. Bhattacharya and M. Pedram, "Short-circuit current behaviour in advanced-node static latches," IEEE Trans. CAS-I, vol. 67, no. 9, pp. 2863-2874, 2020.

[6] J. Choi, H. Lee, and D. Sylvester, "Variation-aware sequential cell design in FinFET technologies," IEEE Trans. Electron Devices, vol. 68, no. 12, pp. 6031-6040, 2021.

[7] K. Raman and R. K. Sharma, "Compact static flip-flops for low-power digital cores," Microelectronics Journal, vol. 112, p. 105040, 2021.

[8] P. Rao and V. Mohanty, "Analysis of overlap power in area-optimized static flip-flops," Integration, the VLSI Journal, vol. 82, pp. 147-156, 2022.

[9] L. Martins and J. Pineda de Gyvez, "Conditional-evaluation sequential circuits for activity-aware digital systems," IEEE Access, vol. 10, pp. 122110-122123, 2022.

[10] S. Gopal and T. Ravi, "Stability limits of semi-dynamic flip-flops under near-threshold operation," IEEE Trans. VLSI Syst., vol. 31, no. 4, pp. 513-526, 2023.

[11] N. Das and B. Xu, "Low-delay pulse-triggered flip-flops with compact pulse generators," Journal of Circuits, Systems and Computers, vol. 32, no. 3, 2350041, 2023.

[12] Y. Tao and K. Fukuda, "Pulse-width robustness in pulse-clocked flip-flops for scaled CMOS," IEEE Trans. CAS-II, vol. 70, no. 8, pp. 3021-3025, 2023.

[13] H. Singh and S. Mittal, "Energy-efficient dual-edge triggered flip-flops for low-voltage digital logic," Microelectronics Reliability, vol. 146, 115154, 2024.

[14] M. Lin and Z. Chen, "Clock-controlled static flip-flops with internal contention suppression," IEEE Trans. Circuits Syst. I, vol. 71, no. 1, pp. 55-66, 2024.

[15] W. Park and K. Jeong, "Selective-gating latch designs for reduced overlap current," IEEE Trans. VLSI Syst., vol. 32, no. 2, pp. 317-329, 2024.

[16] Q. Li and A. Kuznetsov, "Contention-aware dynamic storage elements for energy-constrained edge processors," IEEE Access, vol. 12, pp. 98765-98778, 2024.

[17] Z. Wang, P. Zhao, T. Springer, C. Zhu, J. Mau, A. Wells, Y. Xia, and L. Wang, "Low-power redundant-transition-free TSPC dual-edge triggering flip-flop using single-transistor-clocked buffer," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 31, no. 5, pp. 706-710, May 2023.

[18] A. Bonetti, A. Teman, and A. Burg, "An overlap-contention free true single-phase clock dual-edge-triggered flip-flop," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), May 2015, pp. 1850-1853.

[19] Y. K. Maheshwari and M. Sachdev, "Low-Power, Low-Energy, Static, Contention-Free, TSPC Dual-Edge Triggered Flip-Flops," IEEE Access, vol. 13, pp. 66040-66050, 2025. doi: 10.1109/ACCESS.2025.3560850.

[20] N. Venkata Rao, M. Ramesh, and P. Srinivas, "Comparative Analysis of NAND Gate and D Flip-Flop in Terms of Delay and Power Using Advanced Technology Nodes," International Journal of Innovative Research in Technology, vol. 8, no. 3, pp. 120-125, 2022.

[21] Ch. Jaya Prakash, P. Manoj Kumar, and K. Sai Teja, "Design and Analysis of 18 nm FinFET Based 4-bit Shift Registers Using Transitional Hybrid Logic Flip-Flop," SSRG International Journal of Electrical and Electronics Engineering, vol. 12, no. 1, pp. 15-23, 2025.

[22] Mohammed Sabeeha, K. S. Varun, and B. L. Prasad, "A Low-Power Pass-Logic Flip-Flop Architecture in 18 nm FinFET Technology," International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, vol. 10, no. 5, pp. 47-54, 2021.